

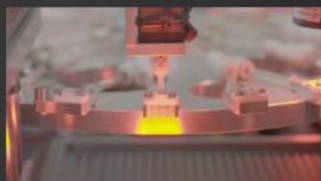
SCTF[®]



差分输出 振荡器

SPXO

值得信赖的专业频率控制元件制造商



www.sctf-crystal.com

值得信赖的专业频率控制元件制造商



企业简介

Company introduction

Since 2003

专业研发、生产、销售系列石英晶体及振荡器产品

推行国际标准质量管理体系：ISO9001:2015、ISO14001: 2015、IATF16949: 2016

国家高新技术企业、专精特新企业、创新型中小型企业

符合ROHS、REACH标准

以客户为中心 视质量为生命

提供晶振及周边电路运用解决方案



SCTF 深圳市星通时频电子有限公司
SHENZHEN SCTF ELECTRONICS CO.,LTD

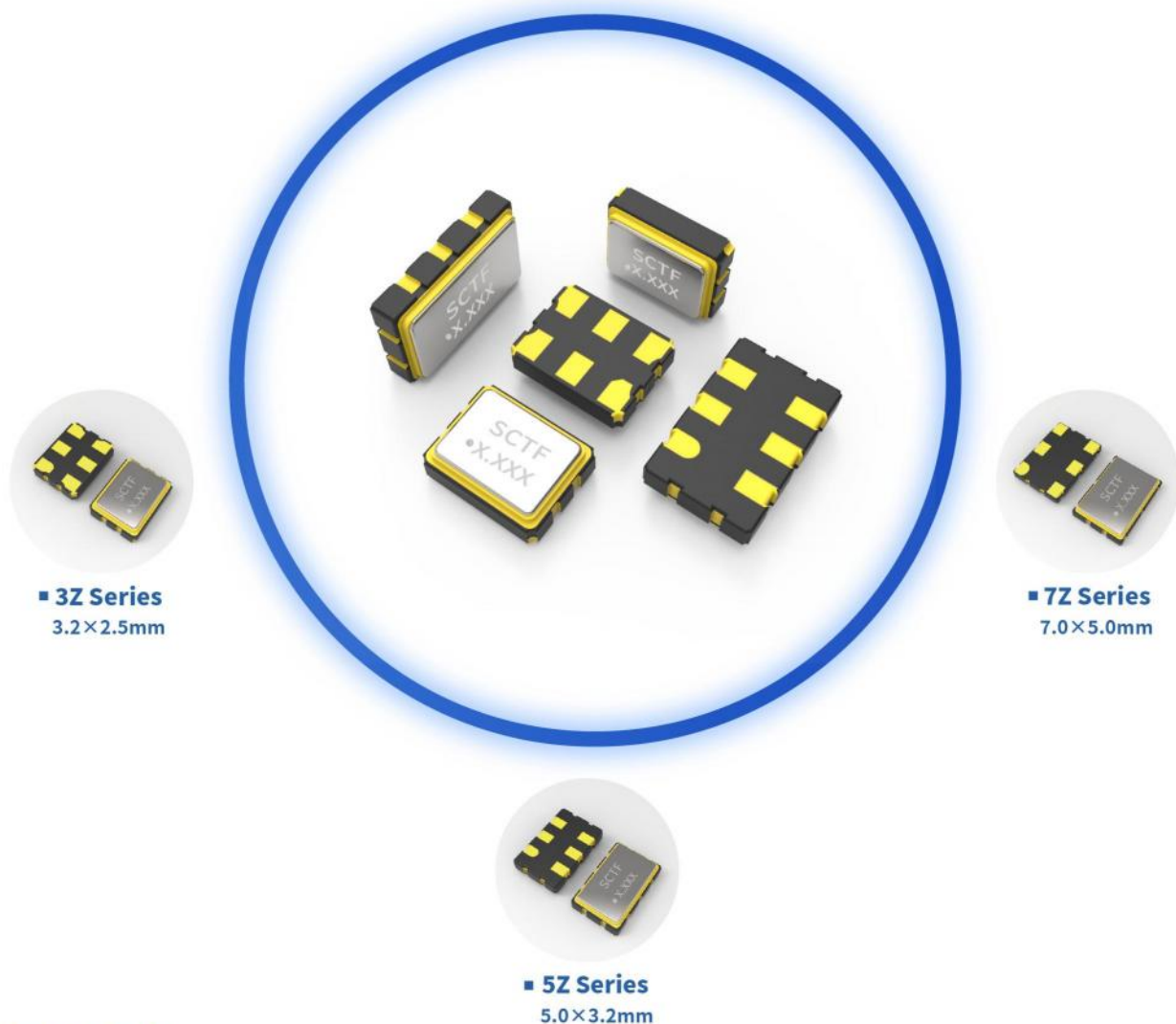
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0755-86097105

sales@sctf-crystal.com

产品外观

Product Appearance



产品结构

Product Structure



产品选型指南

Product Selection Guide

Item Series	Size [mm]		Frequency Range [MHz]	Supply Voltage [Typ.V]	Output	Frequency Tolerance [@25°C; ±ppm]	Frequency Drift [±ppm]	Operating Temperature
	L	W						
3Z	3.2	2.5	90 ~ 160	1.8	LVPECL	10 20	15 20 30	-20°C~+70°C -40°C~+85°C
5Z	5.0	3.2		2.5	LVDS			
7Z	7.0	5.0		3.3	HCSL			

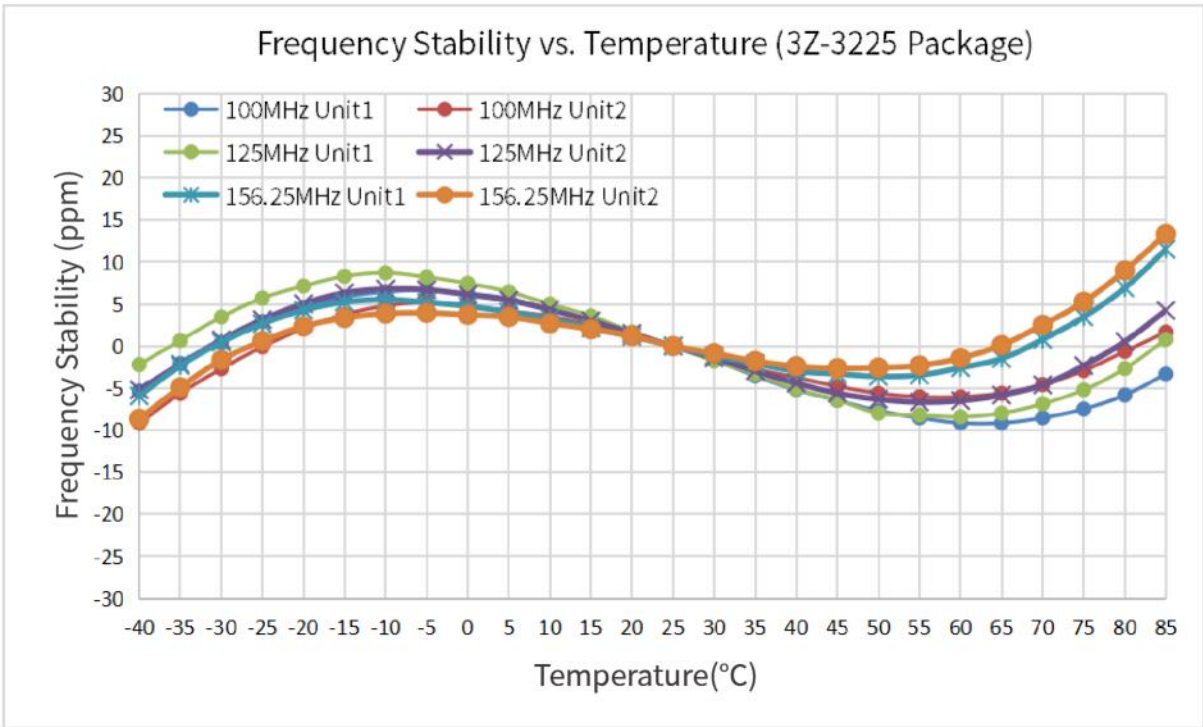
若需要更详细的资料请查询详细规格书或和我们的技术人员联系。

- 1. 选择需要的封装规格及产品系列：3.2×2.5mm; 3Z Series
- 2. 选择需要的频率：100.000MHz
- 3. 选择需要的工作电压：3.3V
- 4. 选择需要的输出模式：LVDS
- 5. 选择需要的频率稳定度 (@+25°C)：±20ppm
- 5. 选择需要的工作温度范围：-40°C ~ +85°C
- 7. 选择需要的频率&温度特性：±30ppm

您需要的产品是：3Z Series 100.000MHz 3.3V ±20ppm@25°C ±30ppm@ -40°C~+85°C

频率温度特性曲线

Frequency Temperature Characteristics



零部件编码示意

Options and Part Identification

Options and Part Identification : Example SX3DF100.000B20F30DNN

Company	Ceramic Package	Frequency Code [MHZ]	Supply Voltage	Frequency Tolerance	Operating Temperature	Frequency Drift	Output	Current Consumption	Phase Noise
SX	3DF	X.XXX	B	20	F	30	D	N	N
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
Code Company		Frequency		Code Frequency Tolerance		Code Frequency Drift		Code Current	
SX SCTF		100.000		10 ±10ppm		15 ±15ppm		N Standard	
				20 ±20ppm		20 ±20ppm			
						30 ±30ppm			
	↓		↓		↓		↓		↓
	Code Ceramic Package		Code Voltage		Code Operating Temperature		Code Output		Code Phase Noise
	7DF 7.0×5.0×1.45mm		D 1.8V		E -20°C ~ +70°C		P LVPECL		N Standard
	5DF 5.0×3.2×1.25mm		H 2.5V		F -40°C ~ +85°C		D LVDS		
	3DF 3.2×2.5×0.9mm		B 3.3V				H HCSL		

If you have other parameter requirements, you can contact **SCTF** at any time.

3Z Series

3.2 x 2.5 mm Differential Output Crystal Oscillator

Feature

- Output Types: LVPECL/LVDS/HCSL
- Tri-state function available
- Low Phase Jitter : 0.5pSec max.
- Pb-free/RoHS Compliant

Applications

- Networking and communications
- Gigabit Ethernet
- Fibre Channel
- SONET/SDH

Frequency Stability & Operating Temperature Range

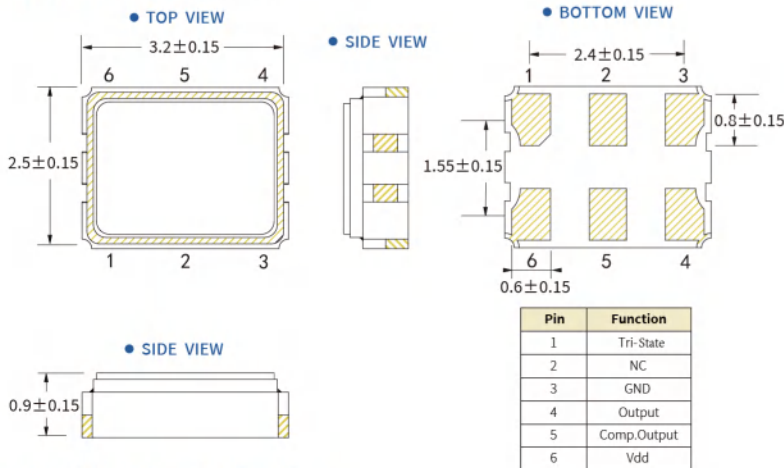
Temp.	FT	±20ppm	±25ppm	±30ppm	±50ppm
-20°C to +70°C	△	★	★	★	★
-40°C to +85°C		△	★	★	★

★: Available △: Conditional

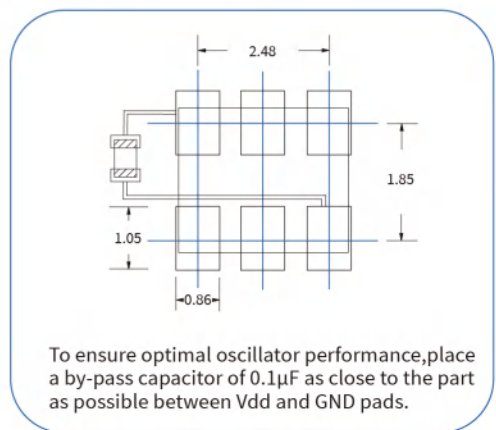
All condition: Include 25°C tolerance, operating temperature range, input voltage change, aging, load change.



Dimensions (UNIT:mm)



Solder pad layout (UNIT:mm)



Electrical Specifications

Item	Symb.	Min.	Typ.	Max.	Unit	Notes
Frequency Range	Freq.	90.000		160.000	MHz	
Standard Frequency	Freq.	100.000, 106.250, 125.000 148.500, 150.000, 155.520 156.250			MHz	Contact SCTF for frequencies not listed
Output		LVPECL				
Operating Temperature	T _{use}	-20		+70	°C	
		-40		+85	°C	
Storage Temperature Range	T _{stg}	-55		+125	°C	
Supply Voltage	Vdd	1.8 / 2.5 / 3.3			V	±5% max.
Output Load	L _{PECL}		50		Ω	Vdd - 2.0 V
Current Consumption	I _{cc}			50	mA	90MHz ≤ Freq. < 125MHz
				75		125MHz ≤ Freq. ≤ 160MHz
Duty Cycle	SYM	45		55	%	
Rise / Fall Time	T _R / T _F			1	nS	20% Vdd to 80% Level
Start-up Time	T _{str}			10	mS	To 90% of Final Amplitude
High output voltage	V _{OH}	Vdd-1.025			V	
Low output voltage	V _{OL}			Vdd-1.62	V	
Enable Voltage High (Logic 1)	V _{IH}	0.7Vdd			V	Pin 1 Tri-state Outputs will be enable if OE is Logic 1 or open; Outputs will be disable if OE is Logic 0.
Enable Voltage Low (Logic 0)	V _{IL}			0.3Vdd	V	
RMS Phase Jitter	T _{RPJ}			0.5	pSec	Period Jitter(12KHz-20MHz)
Phase Noise@156.25MHz	100 Hz		-90		dBc/Hz	
	1 KHz		-120		dBc/Hz	
	10 KHz		-140		dBc/Hz	
Aging	f _{age}			3	ppm	1st. Year at 25°C

Item	Symb.	Min.	Typ.	Max.	Unit	Notes
Frequency Range	Freq.	90.000		160.000	MHz	
Standard Frequency	Freq.	100.000 ,106.250 ,125.000 148.500 ,150.000 ,155.520 156.250			MHz	Contact SCTF for frequencies not listed
Output		LVDS				
Operating Temperature	T _{use}	-20		+70	°C	
		-40		+85	°C	
StorageTemperature Range	T _{stg}	-55		+125	°C	
Supply Voltage	Vdd	1.8 / 2.5 / 3.3			V	±5% max.
Output Load	L _{LVDS}		100		Ω	
Current Consumption	I _{cc}			30	mA	90MHz ≤ Freq. < 125MHz
				40		125MHz ≤ Freq. ≤ 160MHz
Duty Cycle	SYM	45		55	%	
Rise / Fall Time	T _R / T _F			1	nS	20% Vdd to 80% Level
Start-up Time	T _{str}			10	mS	To 90% of Final Amplitude
High output voltage	V _{OH}			1.6	V	
Low output voltage	V _{OL}	0.9			V	
Enable Voltage High (Logic 1)	V _{IH}	0.7Vdd			V	Pin 1 Tri-state Outputs will be enable if OE is Logic 1 or open; Outputs will be disable if OE is Logic 0.
Enable Voltage Low (Logic 0)	V _{IL}			0.3Vdd	V	
RMS Phase Jitter	T _{RPJ}			0.5	pSec	Period Jitter(12KHz-20MHz)
Phase Noise@156.25MHz	100 Hz			-90	dBc/Hz	
	1 KHz			-120	dBc/Hz	
	10 KHz			-140	dBc/Hz	
Aging	f _{age}			3	ppm	1st. Year at 25°C

Item	Symb.	Min.	Typ.	Max.	Unit	Notes
Frequency Range	Freq.	90.000		160.000	MHz	
Standard Frequency	Freq.	100.000 ,106.250 ,125.000 148.500 ,150.000 ,155.520 156.250			MHz	Contact SCTF for frequencies not listed
Output		HCSL				
Operating Temperature	T _{use}	-20		+70	°C	
		-40		+85	°C	
StorageTemperature Range	T _{stg}	-55		+125	°C	
Supply Voltage	Vdd	1.8 / 2.5 / 3.3			V	±5% max.
Output Load	L _{HCSL}	R _S =33 , R _L =50			Ω	
Current Consumption	I _{cc}			35	mA	90MHz ≤ Freq. < 125MHz
				40		125MHz ≤ Freq. ≤ 160MHz
Duty Cycle	SYM	45		55	%	
Rise / Fall Time	T _R / T _F			1	nS	20% Vdd to 80% Level
Start-up Time	T _{str}			10	mS	To 90% of Final Amplitude
High output voltage	V _{OH}	0.66			V	
Low output voltage	V _{OL}			0.15	V	
Enable Voltage High (Logic 1)	V _{IH}	0.7Vdd			V	Pin 1 Tri-state Outputs will be enable if OE is Logic 1 or open; Outputs will be disable if OE is Logic 0.
Enable Voltage Low (Logic 0)	V _{IL}			0.3Vdd	V	
RMS Phase Jitter	T _{RPJ}			0.5	pSec	Period Jitter(12KHz-20MHz)
Phase Noise@156.25MHz	100 Hz			-90	dBc/Hz	
	1 KHz			-120	dBc/Hz	
	10 KHz			-140	dBc/Hz	
Aging	f _{age}			3	ppm	1st. Year at 25°C

5Z Series

5.0 x 3.2 mm Differential Output Crystal Oscillator

Feature

- Output Types: LVPECL/LVDS/HCSL
- Tri-state function available
- Low Phase Jitter : 0.5pSec max.
- Pb-free/RoHS Compliant

Applications

- Networking and communications
- Gigabit Ethernet
- Fibre Channel
- SONET/SDH

Frequency Stability & Operating Temperature Range

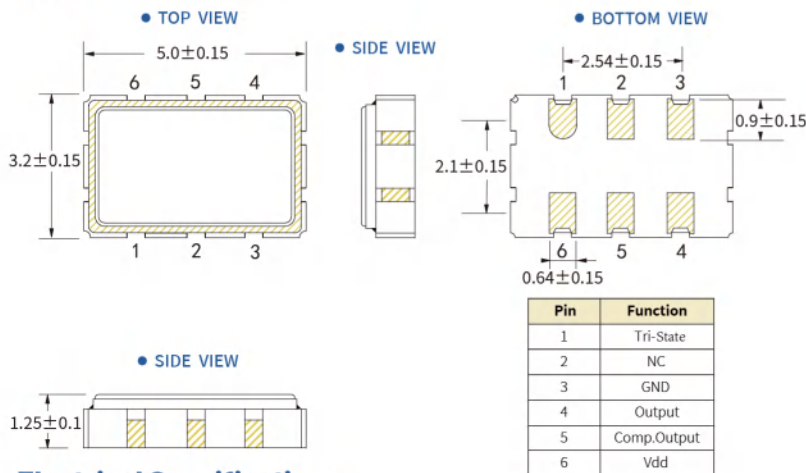
Temp.	FT	±20ppm	±25ppm	±30ppm	±50ppm
-20°C to +70°C	△	★	★	★	★
-40°C to +85°C		△	★	★	★

★: Available △: Conditional

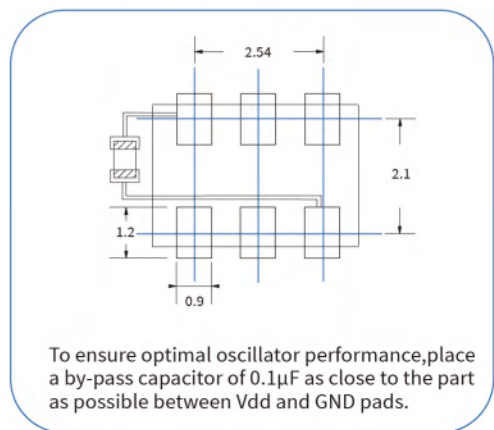
All condition: Include 25°C tolerance, operating temperature range, input voltage change, aging, load change.



Dimensions (UNIT:mm)



Solder pad layout (UNIT:mm)



Electrical Specifications

Item	Symb.	Min.	Typ.	Max.	Unit	Notes
Frequency Range	Freq.	90.000		160.000	MHz	
Standard Frequency	Freq.	100.000, 106.250, 125.000 148.500, 150.000, 155.520 156.250			MHz	Contact SCTF for frequencies not listed
Output		LVPECL				
Operating Temperature	T _{use}	-20		+70	°C	
		-40		+85	°C	
Storage Temperature Range	T _{stg}	-55		+125	°C	
Supply Voltage	Vdd	1.8 / 2.5 / 3.3			V	±5% max.
Output Load	L _{PECL}		50		Ω	Vdd - 2.0 V
Current Consumption	I _{cc}			50	mA	90MHz ≤ Freq. < 125MHz
				75		125MHz ≤ Freq. ≤ 160MHz
Duty Cycle	SYM	45		55	%	
Rise / Fall Time	T _R / T _F			1	nS	20% Vdd to 80% Level
Start-up Time	T _{str}			10	mS	To 90% of Final Amplitude
High output voltage	V _{OH}	Vdd-1.025			V	
Low output voltage	V _{OL}			Vdd-1.62	V	
Enable Voltage High (Logic 1)	V _{IH}	0.7Vdd			V	Pin 1 Tri-state Outputs will be enable if OE is Logic 1 or open; Outputs will be disable if OE is Logic 0.
Enable Voltage Low (Logic 0)	V _{IL}			0.3Vdd	V	
RMS Phase Jitter	T _{RPJ}			0.5	pSec	Period Jitter(12KHz-20MHz)
Phase Noise@156.25MHz	100 Hz		-90		dBc/Hz	
	1 KHz		-120		dBc/Hz	
	10 KHz		-140		dBc/Hz	
Aging	f _{age}			3	ppm	1st. Year at 25°C

Item	Symb.	Min.	Typ.	Max.	Unit	Notes
Frequency Range	Freq.	90.000		160.000	MHz	
Standard Frequency	Freq.	100.000 ,106.250 ,125.000 148.500 ,150.000 ,155.520 156.250			MHz	Contact SCTF for frequencies not listed
Output		LVDS				
Operating Temperature	T _{use}	-20		+70	°C	
		-40		+85	°C	
StorageTemperature Range	T _{stg}	-55		+125	°C	
Supply Voltage	Vdd	1.8 / 2.5 / 3.3			V	±5% max.
Output Load	L_LVDS		100		Ω	
Current Consumption	I _{cc}			30	mA	90MHz ≤ Freq. < 125MHz
				40		125MHz ≤ Freq. ≤ 160MHz
Duty Cycle	SYM	45		55	%	
Rise / Fall Time	T _R / T _F			1	nS	20% Vdd to 80% Level
Start-up Time	T _{str}			10	mS	To 90% of Final Amplitude
High output voltage	V _{OH}			1.6	V	
Low output voltage	V _{OL}	0.9			V	
Enable Voltage High (Logic 1)	V _{IH}	0.7Vdd			V	Pin 1 Tri-state Outputs will be enable if OE is Logic 1 or open; Outputs will be disable if OE is Logic 0.
Enable Voltage Low (Logic 0)	V _{IL}			0.3Vdd	V	
RMS Phase Jitter	T _{RPJ}			0.5	pSec	Period Jitter(12KHz-20MHz)
Phase Noise@156.25MHz	100 Hz		-90		dBc/Hz	
	1 KHz		-120		dBc/Hz	
	10 KHz		-140		dBc/Hz	
Aging	f _{age}			3	ppm	1st. Year at 25°C

Item	Symb.	Min.	Typ.	Max.	Unit	Notes
Frequency Range	Freq.	90.000		160.000	MHz	
Standard Frequency	Freq.	100.000 ,106.250 ,125.000 148.500 ,150.000 ,155.520 156.250			MHz	Contact SCTF for frequencies not listed
Output		HCSL				
Operating Temperature	T _{use}	-20		+70	°C	
		-40		+85	°C	
StorageTemperature Range	T _{stg}	-55		+125	°C	
Supply Voltage	Vdd	1.8 / 2.5 / 3.3			V	±5% max.
Output Load	L_HCSL	R _s =33 , R _L =50			Ω	
Current Consumption	I _{cc}			35	mA	90MHz ≤ Freq. < 125MHz
				40		125MHz ≤ Freq. ≤ 160MHz
Duty Cycle		45		55	%	
Rise / Fall Time	T _R / T _F			1	nS	20% Vdd to 80% Level
Start-up Time	T _{str}			10	mS	To 90% of Final Amplitude
High output voltage	V _{OH}	0.66			V	
Low output voltage	V _{OL}			0.15	V	
Enable Voltage High (Logic 1)	V _{IH}	0.7Vdd			V	Pin 1 Tri-state Outputs will be enable if OE is Logic 1 or open; Outputs will be disable if OE is Logic 0.
Enable Voltage Low (Logic 0)	V _{IL}			0.3Vdd	V	
RMS Phase Jitter	T _{RPJ}			0.5	pSec	Period Jitter(12KHz-20MHz)
Phase Noise@156.25MHz	100 Hz		-90		dBc/Hz	
	1 KHz		-120		dBc/Hz	
	10 KHz		-140		dBc/Hz	
Aging	f _{age}			3	ppm	1st. Year at 25°C

7Z Series 7.0 x 5.0 mm Differential Output Crystal Oscillator

Feature

- Output Types: LVPECL/LVDS/HCSL
- Tri-state function available
- Low Phase Jitter : 0.5pSec max.
- Pb-free/RoHS Compliant

Applications

- Networking and communications
- Gigabit Ethernet
- Fibre Channel
- SONET/SDH

Frequency Stability & Operating Temperature Range

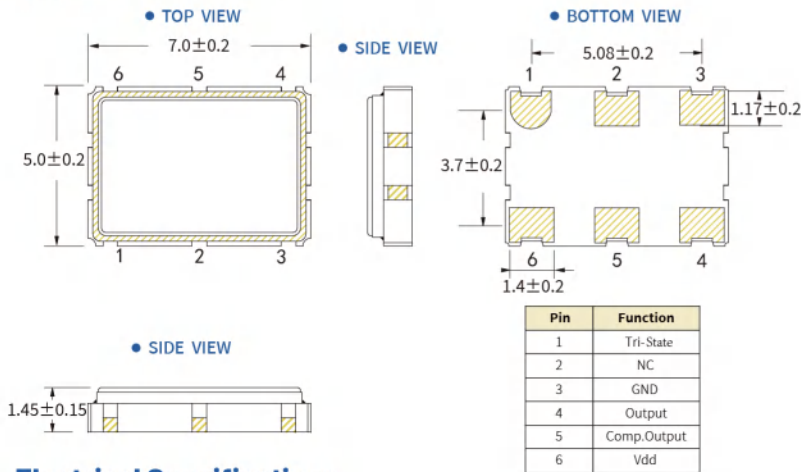
Temp.	FT	±20ppm	±25ppm	±30ppm	±50ppm
-20°C to +70°C	△	★	★	★	★
-40°C to +85°C		△	★	★	★

★: Available △: Conditional

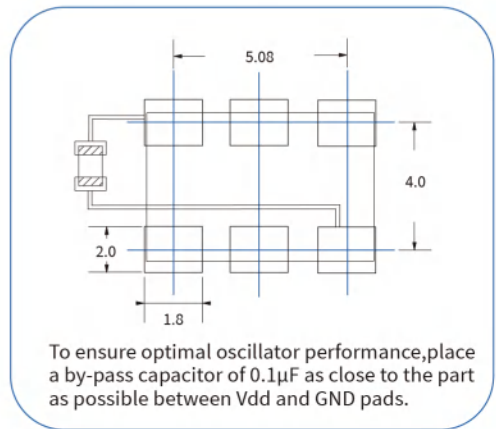
All condition: Include 25°C tolerance, operating temperature range, input voltage change, aging, load change.



Dimensions (UNIT:mm)



Solder pad layout (UNIT:mm)



Electrical Specifications

Item	Symb.	Min.	Typ.	Max.	Unit	Notes
Frequency Range	Freq.	90.000		160.000	MHz	
Standard Frequency	Freq.	100.000, 106.250, 125.000 148.500, 150.000, 155.520 156.250			MHz	Contact SCTF for frequencies not listed
Output		LVPECL				
Operating Temperature	T _{use}	-20		+70	°C	
		-40		+85	°C	
Storage Temperature Range	T _{stg}	-55		+125	°C	
Supply Voltage	Vdd	1.8 / 2.5 / 3.3			V	±5% max.
Output Load	L _{PECL}		50		Ω	Vdd - 2.0 V
Current Consumption	I _{cc}			50	mA	90MHz ≤ Freq. < 125MHz
				75		125MHz ≤ Freq. ≤ 160MHz
Duty Cycle	SYM	45		55	%	
Rise / Fall Time	T _R / T _F			1	nS	20% Vdd to 80% Level
Start-up Time	T _{str}			10	mS	To 90% of Final Amplitude
High output voltage	V _{OH}	Vdd-1.025			V	
Low output voltage	V _{OL}			Vdd-1.62	V	
Enable Voltage High (Logic 1)	V _{IH}	0.7Vdd			V	Pin 1 Tri-state Outputs will be enable if OE is Logic 1 or open; Outputs will be disable if OE is Logic 0.
Enable Voltage Low (Logic 0)	V _{IL}			0.3Vdd	V	
RMS Phase Jitter	T _{RPJ}			0.5	pSec	Period Jitter(12KHz-20MHz)
Phase Noise@156.25MHz	100 Hz		-90		dBc/Hz	
	1 KHz		-120		dBc/Hz	
	10 KHz		-140		dBc/Hz	
Aging	f _{age}			3	ppm	1st. Year at 25°C

Item	Symb.	Min.	Typ.	Max.	Unit	Notes
Frequency Range	Freq.	90.000		160.000	MHz	
Standard Frequency	Freq.	100.000 ,106.250 ,125.000 148.500 ,150.000 ,155.520 156.250			MHz	Contact SCTF for frequencies not listed
Output		LVDS				
Operating Temperature	T _{use}	-20		+70	°C	
		-40		+85	°C	
StorageTemperature Range	T _{stg}	-55		+125	°C	
Supply Voltage	Vdd	1.8 / 2.5 / 3.3			V	±5% max.
Output Load	L_LVDS		100		Ω	
Current Consumption	Icc			30	mA	90MHz ≤ Freq. < 125MHz
				40		125MHz ≤ Freq. ≤ 160MHz
Duty Cycle	SYM	45		55	%	
Rise / Fall Time	T _R / T _F			1	nS	20% Vdd to 80% Level
Start-up Time	T _{str}			10	mS	To 90% of Final Amplitude
High output voltage	V _{OH}			1.6	V	
Low output voltage	V _{OL}	0.9			V	
Enable Voltage High (Logic 1)	V _{IH}	0.7Vdd			V	Pin 1 Tri-state Outputs will be enable if OE is Logic 1 or open; Outputs will be disable if OE is Logic 0.
Enable Voltage Low (Logic 0)	V _{IL}			0.3Vdd	V	
RMS Phase Jitter	T _{RPJ}			0.5	pSec	Period Jitter(12KHz-20MHz)
Phase Noise@156.25MHz	100 Hz		-90		dBc/Hz	
	1 KHz		-120		dBc/Hz	
	10 KHz		-140		dBc/Hz	
Aging	f _{age}			3	ppm	1st. Year at 25°C

Item	Symb.	Min.	Typ.	Max.	Unit	Notes
Frequency Range	Freq.	90.000		160.000	MHz	
Standard Frequency	Freq.	100.000 ,106.250 ,125.000 148.500 ,150.000 ,155.520 156.250			MHz	Contact SCTF for frequencies not listed
Output		HCSL				
Operating Temperature	T _{use}	-20		+70	°C	
		-40		+85	°C	
StorageTemperature Range	T _{stg}	-55		+125	°C	
Supply Voltage	Vdd	1.8 / 2.5 / 3.3			V	±5% max.
Output Load	L_HCSL	R _s =33 , R _L =50			Ω	
Current Consumption	Icc			35	mA	90MHz ≤ Freq. < 125MHz
				40		125MHz ≤ Freq. ≤ 160MHz
Duty Cycle	SYM	45		55	%	
Rise / Fall Time	T _R / T _F			1	nS	20% Vdd to 80% Level
Start-up Time	T _{str}			10	mS	To 90% of Final Amplitude
High output voltage	V _{OH}	0.66			V	
Low output voltage	V _{OL}			0.15	V	
Enable Voltage High (Logic 1)	V _{IH}	0.7Vdd			V	Pin 1 Tri-state Outputs will be enable if OE is Logic 1 or open; Outputs will be disable if OE is Logic 0.
Enable Voltage Low (Logic 0)	V _{IL}			0.3Vdd	V	
RMS Phase Jitter	T _{RPJ}			0.5	pSec	Period Jitter(12KHz-20MHz)
Phase Noise@156.25MHz	100 Hz		-90		dBc/Hz	
	1 KHz		-120		dBc/Hz	
	10 KHz		-140		dBc/Hz	
Aging	f _{age}			3	ppm	1st. Year at 25°C